Self-Powered energy harvester strain sensing device for structural health monitoring

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A. Álvarez[1], M. Bafleur[2], J-M. Dilhac[2], J. Colomer[1], D.Dragomirescu[2], J.Lopez[1], M.Zhu[3] and P. Miribel[1]

[1] Engineering Department: Electronics, Physics Faculty, Martí i Franqués, 1, 08028 Barcelona, Spain
[2] LAAS-CNRS, Université de Toulouse, CNRS, INSA, Toulouse, France
[3] College of Engineering, Mathematics and Physical Sciences, Harrison Building, University of Exeter, Exeter, EX4, 4QF, UK

aalvarez@el.ub.edu

Abstract. This paper presents an envisaged autonomous strain sensor device, which is dedicated to structural health monitoring applications. The paper introduces the ASIC approach that replaces the discrete approach of some of the main modules.

1. Introduction

The proposed device is developed in the frame of the SMARTER (Smart Multifunctional Architecture & Technology for Energy-Aware wireless sensor) Project [1].

The device is self-powered, based on a piezoelectric transducer as an energy-harvesting source, enabling a battery-free solution. The system would be capable to sense the mechanical strain, which is an interesting topic in structural health monitoring applications, particularly in the aerospace field, which is the present field of application, defining the frequencies available for the transducer, harvesting the energy provided by the in-flight vibration of the aircraft's wing [2].

The nice approach of the device, which defines its Multifunctional concept, is that the same transducer used to harvest energy also allows extracting the mechanical strain. On the one hand, based on a piezoelectric transducer, the mechanical vibrations are harvested to generate electrical energy, in order to start-up and supply the system, but on the other hand, the system is capable to extract the open voltage (VOC) of the piezoelectric harvester, which has a relationship with the mechanical strain [3]. Then, based on the open circuit voltage concept to adapt the maximum power transferred condition between the piezoelectric mechanical to electrical energy [4,5,6], a detection of the open voltage of the piezoelectric transducer is derived. Based on these approaches, initial fully discrete electronic solutions have been implemented [7][8] as a proof of concept.

The system is based on four main modules, figure 1: a) the energy transducer as a multifunctional device (MFC) based on a piezoelectric generator (PZT); b) the Power Management, Control and Sensing Circuitry Unit, to be implemented in an ASIC solution (ASIC1); c) the Dynamic Storage Module to store the generated energy (SCap), and d) the Communication (RF) and Data Processing Unit (ASIC2). Full electronics that define the Smarter Device would be placed on a flexible PCB.

In this paper we focus the work regarding the design of ASIC1. This implementation has the role to manage the power harvested, the measurements and the management of the other modules.

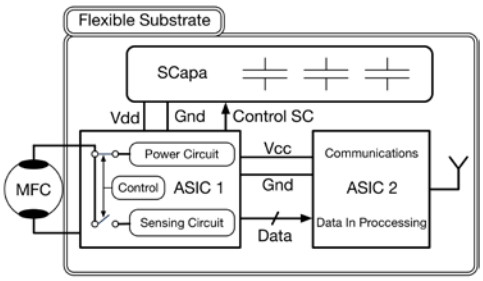

Figure 1. Main blocs for the Smarter Device.

In section 2 is introduced the ASIC1 approach. The initial discrete solutions [7][8] are translated to a microelectronic one, for a more compact solution.

Finally in section 3 are derived some conclusions and future perspectives.

2. Integrated approach

Thanks to the discrete approaches [7,8], the contemplate architecture is validated and with the gained experience we proceeded with the ASIC integration. A first ASIC is going to be implemented based on an AMS 0.35 technology. In figure 2 is depicted the ASIC1 at the functional block level and its layout design in figure 3, in an AMS 0.35µm technology, that will be placed in a QFN32 package.

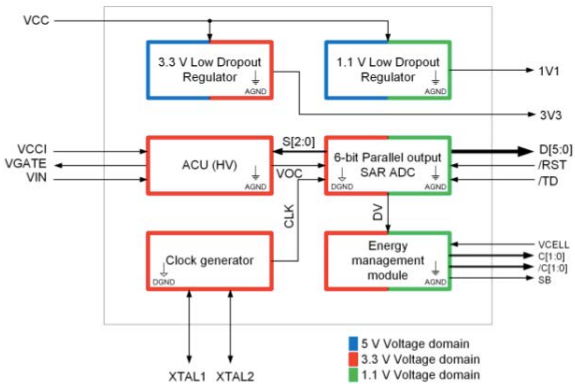

Figure 2. ASIC1's block diagram conception.

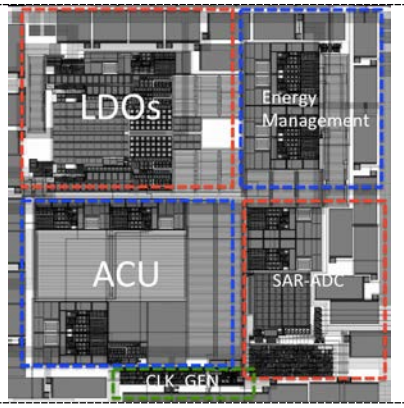

Figure 3. ASIC1 layout implementation.

To interface ASIC1 and ASIC2, figure 1,a communication protocol has been implemented, working with 8 bits: Two bits of control, and 6-bits of data. This protocol is implemented in [8] and validated. In t1 data is available on ASIC1. In t2 ASIC activates Start Bit (SB) when data is ready of transmitting. In ta SB is activated during all operation. In t3 ASIC2 is ready to operate. In tb, the bit Transmission Done (TD) is activated during UR-UWB transmission. In t4 TD is grounded when the transmission is completed. In t5 SB is turned off after communication is done. Finally, in t6 the system waits till new data is available on ASIC1.

The system is focused into the extraction of the strain through VOC, and the validation of the architecture that will combine the electronics envisaged in ASIC1 with those of ASIC2. The wireless solution implemented in [7] will be replaced by ASIC2 in the future Smarter prototype, and ASIC1 has a Data Processing Unit, based on a 6-bits SAR-ADC converter, which prepares the data to be sent by the RF module (ASIC2) replacing the TI Microcontroller in [8]. The strain is measured and related with the open circuit voltage, and the measurement is outputted by 6- parallel bit ADC, which

translates the measurement to the Communication. The main blocs are defined by the Power Circuit Unit, which combines linear regulators and the Energy Management module. The system needs a 1.1V regulated voltage source and a 3.3V regulated voltage source. From the AC/DC rectifier two LDOs will generate these voltages. The 1.1V LDO is designed to bias ASIC2, and the 3.3V LDO to bias the rest of the electronics. Then, the Energy Management module has the role to control the Dynamic Storage Element or SCap [9]. Finally, the ACU module and the 6-bit SAR ADC Converter define the Control Circuit and Sensing Circuitry.

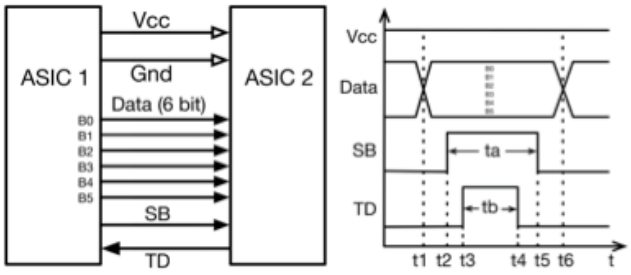

Figure 4. Communication protocol between ASICS.

The Power Circuit Unit is described more in detail. A specific low-power bandgap reference and current reference circuit has been designed; with a current consumption lower than 9μA, nominally and a nominal power consumption of 30μW. It has the capability to work from a lower voltage of 2V till 5V, the maximum operating voltage, with an output voltage of 1.23V with a Temperature Coefficient (TC) lower than 60ppm. The current reference is 105nA with a TC lower than 250ppm, in the temperature range of -40ºC to 125 ºC.

Then, based on the architectures presented in [5], the LDO circuits have been designed. The 3.3V LDO is designed to work with a current up to 1mA, and the 1.1V LDO with a maximum DC current of 10mA. The main parameters for the LDO are introduced. In the case of the 3.3V LDO the Linear Regulation is $68.7 \cdot 10^{-3}$ (V/V). In the case of the 1.1V LDO is $665 \cdot 10^{-9}$(V/V). The ability to maintain the output voltage with variations of the input voltage is reasonable for both designs. The measurement of the capability of the circuitry to keep the regulated output voltage to the desired value against changes of the load, that is, between light and high load conditions (in our case between few μA that define the quiescent operating point of the electronics and the load condition of 1mA for the 3.3V LDO and 10mA for the 1.1V LDO), is the load regulation, which is $81.6 \cdot 10^{-3}$ (V/A) in the case of the 3.3V LDO and $99 \cdot 3 \cdot 10^{-6}$ (V/A) for the 1.1V LDO regulator.

Full Monte Carlo analyses have been carried out for the bandgap reference circuit and LDOs. In the particular case of the Linear Dropout Regulators, it is the 1.1V LDO that has the greater limitation, with an accepted range between 1.05 and 1.18V, with 200 samples. The average regulated voltage is 1.12V with a standard deviation of 34,19 mV (Yield of 95%).

The ACU module, which is quite complex, and the Energy management module, are out of the scope of the present work. In figure 5 is depicted the caption of the simulation, at the extracted ASIC view level, of the performance of the ACU control stage though the GATE signal (VGATE) [7][8].

3. Conclusions

This paper presents the ASIC approach for the power management, control and sensing for the SMARTER project. Future full test and characterization will be carried out before its implementation in the final prototype on flexible substrate and reported in future publications.

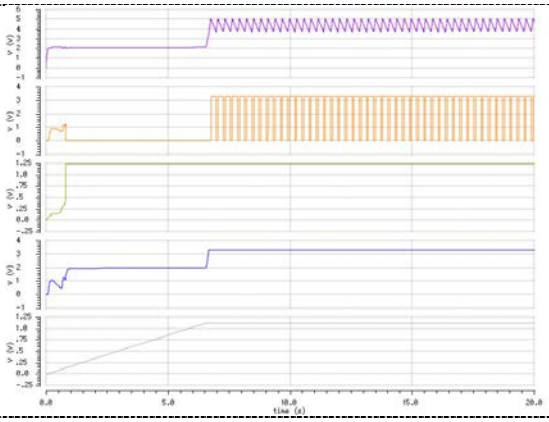

Figure 5. Caption of the transient simulation, from the ASIC1 extracted view, of the GATE control signal. Generation of the scenario operating phases. From the Top view to the bottom caption: (Top) Start-Up and harvest/measuring phases; VGATE signal that control the phases; Bandgap reference voltage; 3V3 LDO regulated voltage; (bottom) 1V1 LDO regulated voltage.

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